



# Low-Voltage, Low $r_{ON}$ , Dual DPDT Analog Switch

## FEATURES

- Low Voltage Operation (2.7 V to 3.3 V)
- Low On-Resistance -  $r_{ON}$ : 0.85  $\Omega$
- 3 dB Loss @ 100 MHz
- Fast Switching:  $t_{ON}$  = 40 ns  
 $t_{OFF}$  = 35 ns
- QFN-16 Package

## BENEFITS

- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- TTL/1.8-V Logic Compatible
- High Bandwidth

## APPLICATIONS

- Cellular Phones
- Speaker Headset Switching
- Audio and Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems

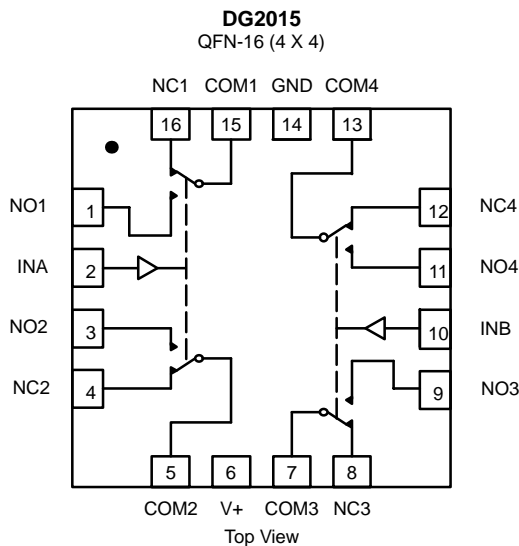
## DESCRIPTION

The DG2015 is a dual double-pole/double-throw monolithic CMOS analog switch designed for high performance switching of analog signals. Combining low power, high speed, low on-resistance and small physical size, the DG2015 is ideal for portable and battery powered applications requiring high performance and efficient use of board space.

The DG2015 is built on Vishay Siliconix's low voltage J12 process. An epitaxial layer prevents latchup. Break-before-make is guaranteed.

The switch conducts equally well in both directions when on, and blocks up to the power supply level when off.

## FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	NC1, 2, 3 and 4	NO1, 2, 3 and 4
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85°C	16-Pin QFN (4 x 4 mm)	DG2015DN

**ABSOLUTE MAXIMUM RATINGS**

Reference to GND

V+	-0.3 to +6 V
IN, COM, NC, NO <sup>a</sup>	-0.3 to (V+ + 0.3 V)
Current (Any terminal except NO, NC or COM)	30 mA
Continuous Current (NO, NC, or COM)	± 150 mA
Peak Current (Pulsed at 1 ms, 10% duty cycle)	± 200 mA
Storage Temperature (D Suffix)	-65 to 150°C
Package Solder Reflow Conditions <sup>d</sup>	
16-Pin QFN (4 x 4 mm)	240°C

Power Dissipation (Packages)<sup>b</sup>

QFN-16 <sup>c</sup>	1880 mW
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- Notes:
- Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
  - All leads welded or soldered to PC Board.
  - Derate 23.5 mW/°C above 70°C
  - Manual soldering with iron is not recommended for leadless components. The QFN is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper lip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10%, V <sub>IN</sub> = 0.4 or 2.0 V <sup>e</sup>	Temp <sup>a</sup>	Limits -40 to 85°C			Unit
				Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>Analog Switch</b>							
Analog Signal Range <sup>d</sup>	V <sub>NO</sub> , V <sub>NC</sub> , V <sub>COM</sub>		Full	0		V+	V
On-Resistance	r <sub>ON</sub>	V+ = 2.7 V, V <sub>COM</sub> = 0.2 V/1.5 V, I <sub>NO</sub> , I <sub>NC</sub> = 100 mA	Room Full		0.85	1.6 1.7	Ω
r <sub>ON</sub> Flatness	r <sub>ON</sub> Flatness	V+ = 2.7 V V <sub>COM</sub> = 0 to V+, I <sub>NO</sub> , I <sub>NC</sub> = 100 mA	Room		0.16		
r <sub>ON</sub> Match	Δr <sub>ON</sub>		Room		0.15		
Switch Off Leakage Current	I <sub>NO(off)</sub> , I <sub>NC(off)</sub>	V+ = 3.3 V, V <sub>NO</sub> , V <sub>NC</sub> = 1 V/3 V V <sub>COM</sub> = 3 V/1 V	Room Full	-1 -10		1 10	nA
	I <sub>COM(off)</sub>		Room Full	-1 -10		1 10	
Channel-On Leakage Current	I <sub>COM(on)</sub>	V+ = 3.3 V, V <sub>NO</sub> , V <sub>NC</sub> = V <sub>COM</sub> = 1 V/3 V	Room Full	-1 -10		1 10	
<b>Digital Control</b>							
Input High Voltage	V <sub>INH</sub>		Full	2			V
Input Low Voltage	V <sub>INL</sub>		Full			0.4	
Input Capacitance	C <sub>in</sub>		Full		4		pF
Input Current	I <sub>INL</sub> or I <sub>INH</sub>	V <sub>IN</sub> = 0 or V+	Full	-1		1	μA
<b>Dynamic Characteristics</b>							
Turn-On Time	t <sub>ON</sub>	V <sub>NO</sub> or V <sub>NC</sub> = 2.0 V, R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF	Room Full		40	65 67	ns
Turn-Off Time	t <sub>OFF</sub>		Room Full		35	60 62	
Break-Before-Make Time	t <sub>d</sub>		Full	1	3		
Charge Injection <sup>d</sup>	Q <sub>INJ</sub>	C <sub>L</sub> = 1 nF, V <sub>GEN</sub> = 0 V, R <sub>GEN</sub> = 0 Ω	Room		7		pC
Off-Isolation <sup>d</sup>	OIRR	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz	Room		-67		dB
Crosstalk <sup>d</sup>	X <sub>TALK</sub>		Room		-70		
N <sub>O</sub> , N <sub>C</sub> Off Capacitance <sup>d</sup>	C <sub>NO(off)</sub>	V <sub>IN</sub> = 0 or V+, f = 1 MHz	Room		63		pF
	C <sub>NC(off)</sub>		Room		67		
Channel-On Capacitance <sup>d</sup>	C <sub>NO(on)</sub>		Room		200		
	C <sub>NC(on)</sub>		Room		196		

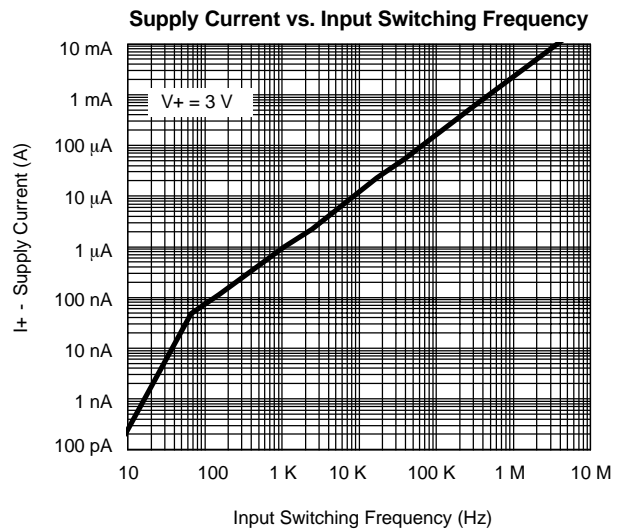
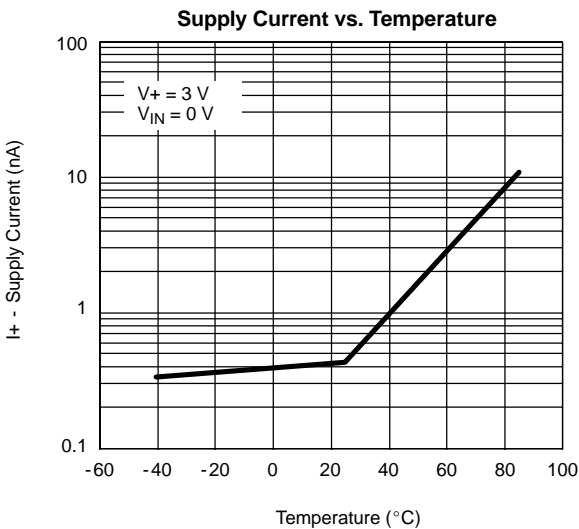
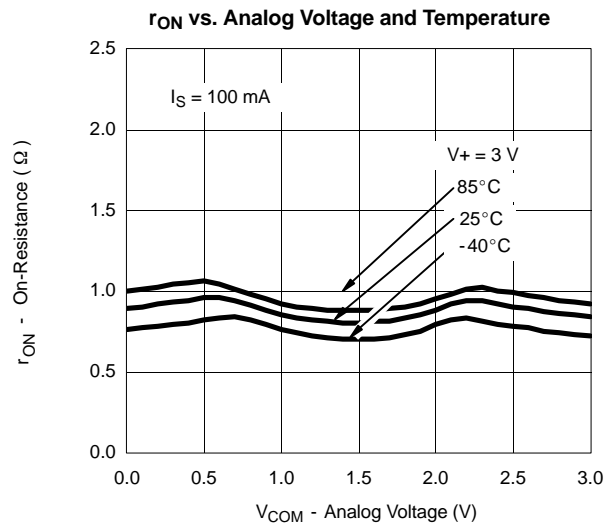
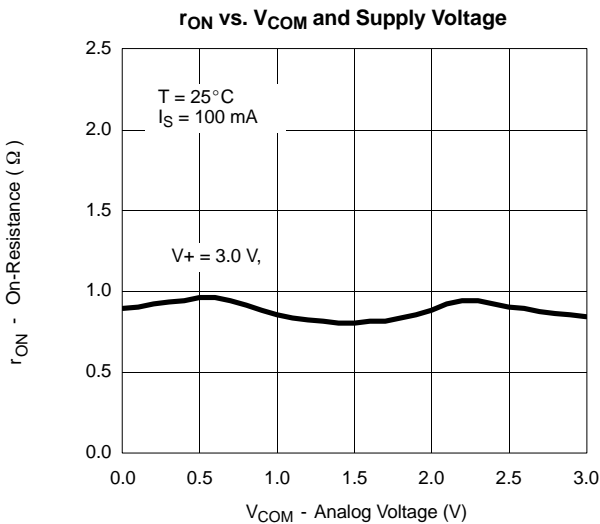


SPECIFICATIONS (V+ = 3 V)							
Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ±10%, VIN = 0.4 or 2.0 V <sup>e</sup>	Temp <sup>a</sup>	Limits -40 to 85°C			Unit
				Min <sup>b</sup>	Typ <sup>c</sup>	Max <sup>b</sup>	
<b>Power Supply</b>							
Power Supply Range	V+			2.7		3.3	V
Power Supply Current	I+	VIN = 0 or V+	Full			1.0	μA
Power Consumption	PC		Full			3.3	μW

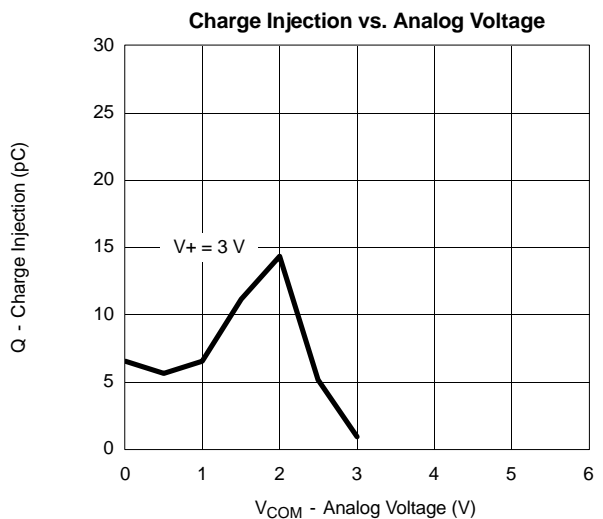
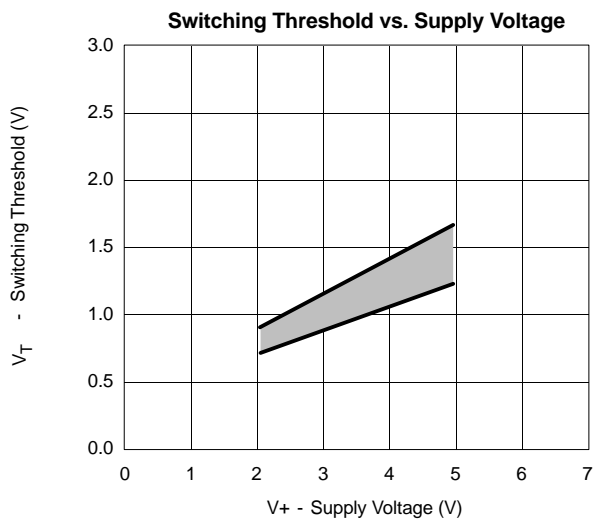
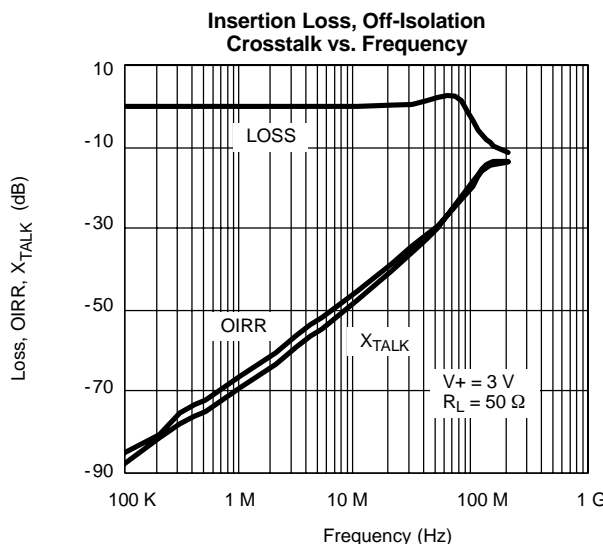
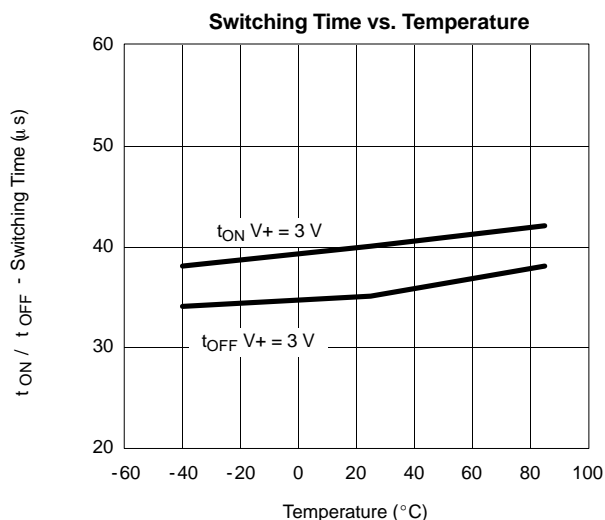
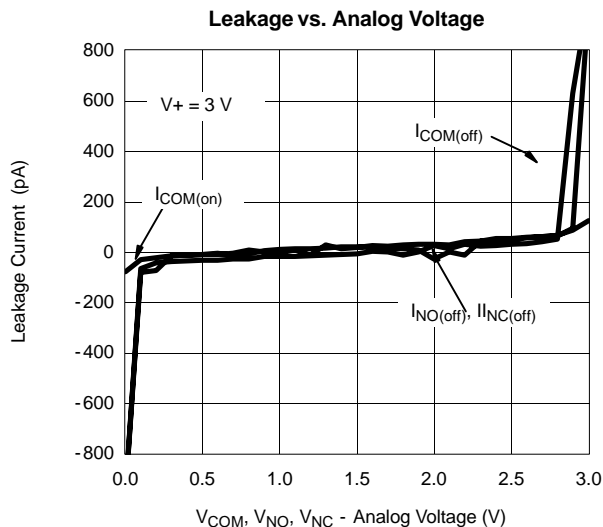
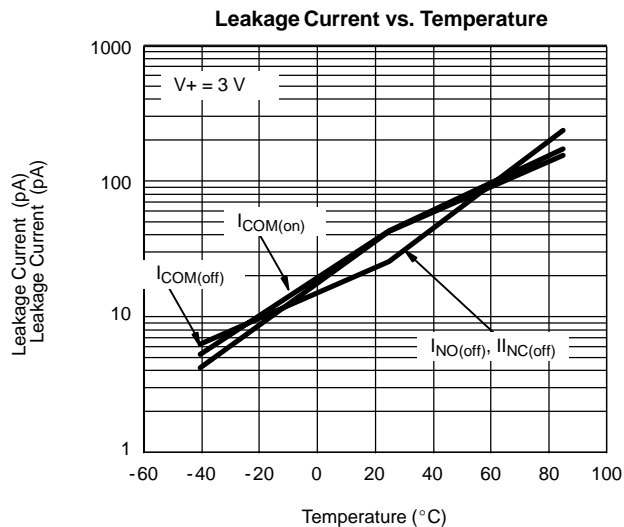
Notes:

- a. Room = 25°C, Full = as determined by the operating suffix.
- b. Typical values are for design aid only, not guaranteed nor subject to production testing.
- c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- d. Guarantee by design, nor subjected to production test.
- e. VIN = input voltage to perform proper function.
- f. Guaranteed by 5-V leakage testing, not production tested.

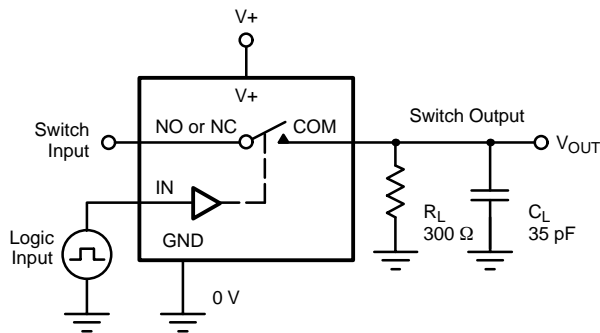
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**



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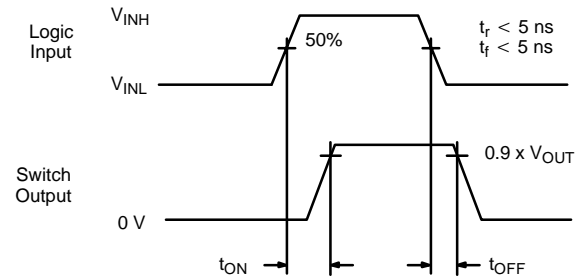


TEST CIRCUITS



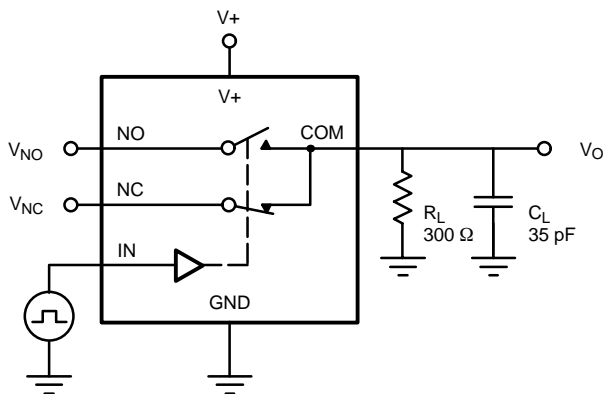
$C_L$  (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left( \frac{R_L}{R_L + R_{ON}} \right)$$



Logic "1" = Switch On  
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time



$C_L$  (includes fixture and stray capacitance)

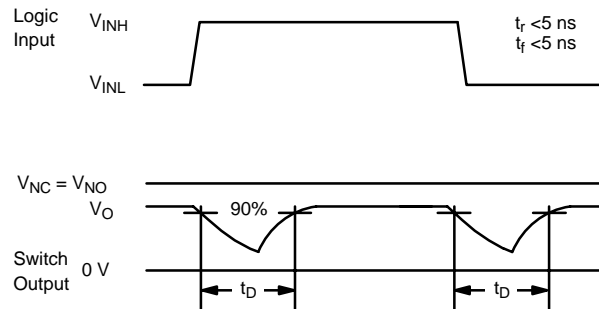
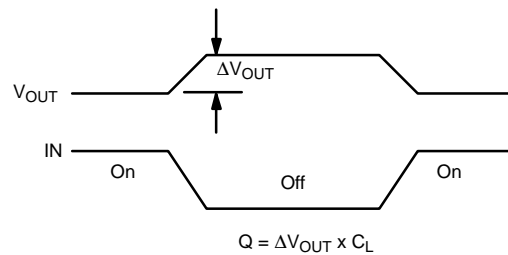
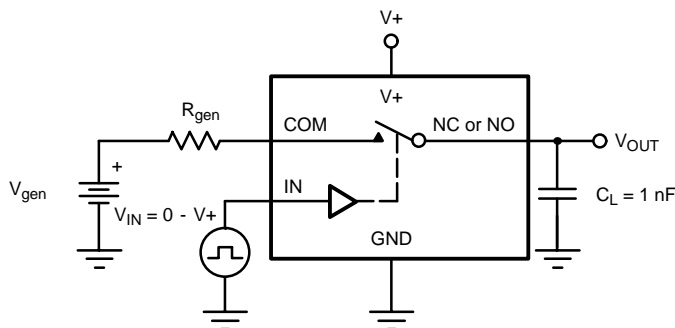


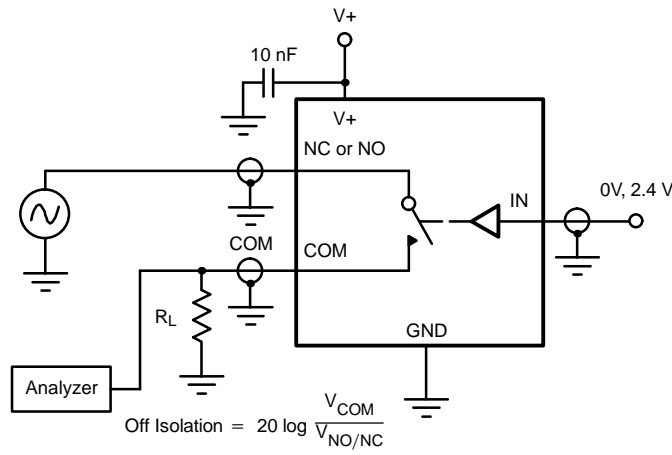
Figure 2. Break-Before-Make Interval



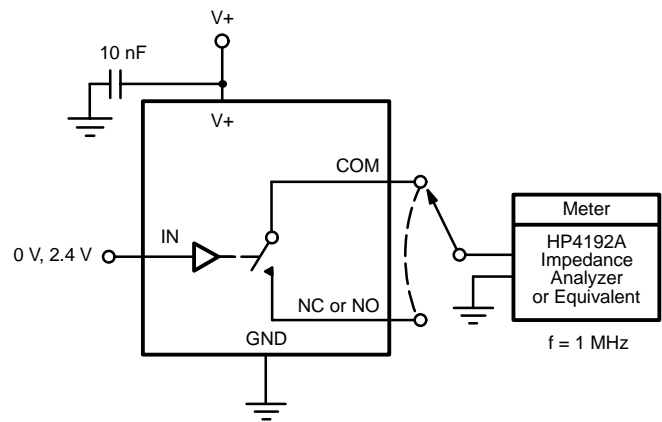
IN depends on switch configuration: input polarity determined by sense of switch.

Figure 3. Charge Injection

**TEST CIRCUITS**



**Figure 4.** Off-Isolation



**Figure 5.** Channel Off/On Capacitance